

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (original): A vertical semiconductor component, comprising:

a substrate of a first conductivity type having a first and a second side;

an insulating layer covering said first side and having a side remote from said substrate;

a more highly doped layer of the first conductivity type applied on said second side;

a metallic drain contact applied on said more highly doped layer;

a metallic gate contact;

a multiplicity of MOS cells on said first side of said substrate for forming a first semiconductor switch, each MOS cell having:

a first well of the second conductivity type, said first well being introduced into said substrate and reaching said first side;

a first metallic source contact extended through said insulating layer;

a first source region of the first conductivity type being incorporated into said well and having a potential, reaching to said first side of said substrate, and connecting to said first metallic source contact;

a first gate on said side of said insulating layer remote from said substrate, said first gate partly covering said well and connecting to said metallic gate contact;

a plurality of further MOS cells identical to said multiplicity of MOS cells, said further MOS cells having a second well , a second source region having a potential, a second gate on said first side of said substrate for forming a second semiconductor switch; and a second source contact electrically insulated from said first source contact and extending through said insulating layer; said second source regions of said further MOS cells connected to said second source contact on said first side; and

a region of the second conductivity type being incorporated into said substrate, reaching to said first side, and electrically connecting to said second gate of said further MOS cells, said region having a potential floating relative to the potential of the first and second source regions of said MOS cells and further MOS cells.

Claim 2 (original): The vertical semiconductor component according to claim 1, wherein said region of the second conductivity type is surrounded exclusively by said further MOS cells, to form a structure for switching on said MOS cells.

Claim 3 (original): The vertical semiconductor component according to claim 2, wherein said switching-on structure is disposed adjacent said MOS cells of said first semiconductor switch.

Claim 4 (original): The vertical semiconductor component according to claim 2, wherein said switching-on structure is surrounded by said MOS cells.

Claim 5 (cancelled).

Claim 6 (original): The vertical semiconductor component according to claim 2, including a lateral insulation provided between said MOS cells and said structure switching on said MOS cells.

Claim 7 (original): The vertical semiconductor component according to claim 1, wherein at least one of said further MOS cells is surrounded exclusively by regions of the second conductivity type, to form a structure for switching on said MOS cells.

Claim 8 (original): The vertical semiconductor component according to claim 7, wherein said switching-on structure is disposed adjacent said MOS cells of said first semiconductor switch.

Claim 9 (original): The vertical semiconductor component according to claim 7, wherein said switching-on structure is surrounded by said MOS cells.

Claim 10 (original): The vertical semiconductor component according to claim 7, including a lateral insulation provided between MOS cells and said structure switching on said MOS cells.

Claim 11 (original): The vertical semiconductor component according to claim 1, wherein:

said region is formed in the direction of said second side and holds a charge; and

a space charge zone is defined between said further MOS cells and said region, said space charge zone propagating the charge and driving said gate of the further MOS cells therewith.

Claim 12 (original): The vertical semiconductor component according to claim 11, wherein said region extends orthogonally from said first side toward said second side.

Claim 13 (original): The vertical semiconductor component according to claim 1, wherein said wells of said MOS cells and further MOS cells extend orthogonally from said first side to said second side.

Claim 14 (original): The vertical semiconductor component according to claim 1, including a plurality of said regions, some of said regions being laterally insulated from said further MOS cells and reaching into said substrate less than said wells of said MOS cells.

Claim 15 (original): The vertical semiconductor component according to claim 1, including a plurality of said regions, some of said regions being laterally insulated from said further MOS cells and doped to create a breakdown voltage less than a breakdown voltage of said MOS cells.

Claim 16 (original): The vertical semiconductor component according to claim 1, wherein the first conductivity type is n-conducting.

Claim 17 (original): The vertical semiconductor component according to claim 1, wherein said further MOS cells are connected in a cascaded manner.

Claim 18 (original): The vertical semiconductor component according to claim 1, wherein said regions are connected in a cascaded manner.

Claim 19 (original): The vertical semiconductor component according to claim 18, wherein said further MOS cells are also connected in a cascaded manner.

Claim 20 (withdrawn): A lateral semiconductor component, comprising:

a first substrate of the first conductivity type having a first and a second side;

an insulating layer covering said first side and having a side remote from said substrate;

a second substrate of the second conductivity type applied on said second side;

a multiplicity of MOS cells on said first side for forming a first semiconductor switch, each MOS cell including:

a first source electrode passing through the insulating layer,

a drain electrode passing through said insulating layer,

a first source region having a potential introduced into said first substrate reaching to said first side and electrically contact-connecting via said first source electrode,

a drain region introduced into said substrate reaching to said first side for electrically contact-connecting via said drain electrode, and

a first gate applied on the side of said insulating layer that is remote from said first substrate and partly covering at least said first source region;

a plurality of further MOS cells , each having a second source region having a potential, being introduced into said substrate and reaching to said first side, a second source electrode passing through said insulating layer, and a second gate at least partly covering said second source region, said second source region can be electrically contact-connected to said second source electrode and at least partly covering said second source region;

a region of the second conductivity type being incorporated into said substrate, reaching to said first side, and electrically connecting to said second gate, said region having a potential floating relative to the potential of said first and second source regions.

Claim 21 (withdrawn): The lateral semiconductor component according to claim 20, wherein at least one of said first and said second source region forms a well of the second conductivity type, said well incorporating a region of the first conductivity type reaching said first side and connecting to a respective source electrode.

Claim 22 (withdrawn): The lateral semiconductor component according to claim 20, wherein said region is surrounded exclusively by said second source regions to form a structure switching on said MOS cells.

Claim 23 (withdrawn): The lateral semiconductor component according to claim 22, including a lateral insulation provided between said MOS cells and said structure switching on said MOS cells.

Claim 24 (withdrawn): The lateral semiconductor component according to claim 22, wherein said structure switching on said MOS cells is adjacent said MOS cells.

Claim 25 (withdrawn): The lateral semiconductor component according to claim 22, wherein said structure switching on said MOS cells is surrounded by said MOS cells.

Claim 26 (withdrawn): The lateral semiconductor component according to claim 20, wherein said second source region is surrounded exclusively by said regions to form a structure switching on said MOS cells.

Claim 27 (withdrawn): The lateral semiconductor component according to claim 26, wherein said structure switching on said MOS cells is adjacent said MOS cells.

Claim 28 (withdrawn): The lateral semiconductor component according to claim 26, wherein said structure switching on said MOS cells is surrounded by the MOS cells.

Claim 29 (withdrawn): The lateral semiconductor component according to claim 26, including a lateral insulation provided between said MOS cells and said structure switching on said MOS cells.

Claim 30 (withdrawn): The lateral semiconductor component according to claim 20, including:

a further region containing a charge and connected to said region; and

a space charge zone defined between the second source region and the region for propagating the charge to drive said second gate.

Claim 30 (withdrawn): The lateral semiconductor component according to claim 29, wherein said further region extends toward said drain electrode in said first substrate.

Claim 31 (withdrawn): The lateral semiconductor component according to claim 30, wherein said further region extends along said first side.

Claim 32 (withdrawn): The lateral semiconductor component according to claim 20, wherein the first conductivity type is n-conducting.

Claim 33 (withdrawn): The vertical semiconductor component according to claim 20, wherein said further MOS cells and/or said regions are connected in a cascaded manner.

Claim 34 (withdrawn): The vertical semiconductor component according to claim 20, wherein said regions are connected in a cascaded manner.

Claim 35 (withdrawn): The vertical semiconductor component according to claim 34, wherein said further MOS cells are also connected in a cascaded manner.